CLAIMS

What is claimed is:

1. An apparatus for processing a semiconductor wafer, comprising:

a processing chamber;

a silylating agent inlet to said processing chamber, said silylating agent inlet configured to provide a silylating agent to the interior of said processing chamber; and

an oxidizing inlet, configured to provide an oxidizing agent to the interior of said processing chamber.

2. The apparatus of Claim 1, further comprising an etch gas inlet, said etch gas inlet configured to provide an etch gas to the interior of said processing chamber.

3. The apparatus of Claim 1, wherein said processing chamber is configured to perform an ashing process followed by a silylating process.

4. The apparatus of Claim 1, wherein said processing chamber is configured to perform a cure process followed by a silylating process.

5. The apparatus of Claim 1, further comprising an etch gas inlet configured to provide an etch gas to the interior of said processing chamber.

6. The apparatus of Claim 5, wherein said processing chamber is configured to perform an etch process, an ashing process, and a silylation process.

7. The apparatus of Claim 1, further comprising a pump port for evacuating said processing chamber.

8. A cluster tool for semiconductor processing, comprising:

an ash/silylation chamber, said ash/silylation chamber configured to perform an ashing process and a silylation process; and

a wafer in/out chamber, configured to introduce one or more wafers into said cluster tool.

9. The cluster tool of Claim 8, further comprising a processing chamber.

10. The cluster tool of Claim 9, wherein said processing chamber comprises a cap deposition module.

11. The cluster tool of Claim 10, wherein said cap deposition module is chosen from the group consisting of a PECVD module and a spin-on deposition module.

12. The cluster tool of Claim 9, wherein said processing chamber comprises an etch module.

13. A cluster tool for semiconductor processing, comprising:

an etch/ash/silylation chamber, said etch/ash/silylation chamber configured to perform an etch process, an ashing process and a silylation process; and

a wafer in/out chamber, configured to introduce one or more wafers into said cluster tool.

14. The cluster tool of Claim 13, wherein said etch/ash/silylating chamber further comprises a processing chamber.

15. The cluster tool of Claim 14, wherein said processing chamber comprises a cap deposition chamber.

16. The cluster tool of Claim 15, wherein said cap deposition chamber is chosen from the group consisting of a PECVD chamber and a spin-on deposition chamber.

17. A cluster tool for semiconductor processing, comprising:

an organic removal/silylation chamber, configured to remove organic sacrificial material from a low-k layer and configured to perform a silylation process; and

a wafer in/out chamber, configured to introduce one or more wafers into said cluster tool.

18. The cluster tool of Claim 17, further comprising a deposition chamber configured to deposit said low-k layer including organic sacrificial material onto one or more wafers.

19. The cluster tool of Claim 18, wherein said deposition chamber is chosen from the group consisting of a PECVD chamber and a spin-on deposition chamber.

20. The cluster tool of Claim 17, further comprising a cap deposition chamber.

21. The cluster tool of Claim 20, wherein said cap deposition chamber is chosen from the group consisting of a PECVD chamber and a spin-on deposition chamber.

22. A method of repairing damage to a low-k dielectric layer, comprising:

providing a low-k dielectric layer;

providing a photoresist layer disposed above at least a portion of said low-k dielectric layer;

removing at least a portion of said photoresist layer using an ashing process; and

subsequently performing a silylating process.

23. The method of Claim 22, wherein said ashing process comprises forming hydrophilic bonds in said low-k dielectric layer.

24. The method of Claim 23, wherein said hydrophilic bonds include Si-OH.

25. The method of Claim 23, wherein said silylating process comprises replacing at least some hydrophilic bonds with hydrophobic bonds.

26. The method of Claim 25, wherein said hydrophobic bonds include Si-O-Si-$(CH_3)_3$ bonds.

27. The method of Claim 25, wherein said hydrophobic bonds include Si-O-Si$(CH_3)_2$-O-Si bonds.

28. The method of Claim 22, wherein said low-k dielectric layer includes a material chosen from the group consisting of aerogel, xerogel, silicalite, dendrite-based porous glass, mesoporous silica, and carbon-doped oxide.

29. The method of Claim 22, wherein said low-k dielectric layer includes a silsesquioxane.

30. The method of Claim 29, wherein said silsesquioxane is chosen from the group consisting of porous methylsilsesquioxane (MSSQ) and hydrisosilsesquioxane (HSQ).

31. The method of Claim 22, wherein said ashing process comprises providing an oxygen plasma to remove said photoresist layer.

32. The method of Claim 22, wherein performing said silylating process comprises providing a silylating agent.

33. The method of Claim 32, wherein said silylating agent is chosen from the group consisting of hexamethyldisilazane (HMDS), dichlorodimethylsilane (DCDMS), chlorotrimethylsilane (CTMS), and acetaldehyde.

34. The method of Claim 22, wherein said ashing process and said silylating process are performed in the same processing chamber.

35. A method of processing a substrate, comprising:

providing said substrate;

forming a low-k dielectric layer disposed above at least a portion of said substrate;

forming a photoresist layer disposed above at least a portion of said low-k dielectric layer;

patterning said photoresist layer;

removing a portion of said photoresist layer according to said patterning;

processing a portion of said low-k dielectric layer according to said patterning;

performing an ashing process to substantially remove remaining portions of said photoresist layer; and

subsequently performing a silylating process.

36. The method of Claim 35 wherein said processing a portion of said low-k dielectric layer comprises etching.

37. The method of Claim 35 wherein said low-k dielectric layer includes a material from the group consisting of aerogel, xerogel, silicalite, dendrite-based porous glass, mesoporous silica, and carbon-doped oxide.

38. The method of Claim 35, wherein said low-k dielectric layer includes a silsesquioxane.

39. The method of Claim 38, wherein said silsesquioxane is chosen from the group consisting of porous methylsilsesquioxane (MSSQ) and hydrisosilsesquioxane (HSQ).

40. The method of Claim 35, wherein performing said silylating process comprises providing a silylating agent from the group consisting of hexamethyldisilazane (HMDS), dichlorodimethylsilane (DCDMS), chlorotrimethylsilane (CTMS), and acetaldehyde.

41. The method of Claim 35, wherein said ashing process comprises providing an oxygen plasma to remove said photoresist layer.

42. The method of Claim 35, wherein said ashing process and said silylating process are performed in the same processing chamber.

43. The method of Claim 35, wherein said ashing process damages at least a portion of said low-k dielectric layer by causing the formation of hydrophilic bonds.

44. The method of Claim 43, wherein said hydrophilic bonds comprise Si-OH bonds.

45. The method of Claim 43, wherein said silylating process repairs at least a portion of said damage to said low-k dielectric layer by replacing at least a portion of said hydrophilic bonds with hydrophobic bonds.

46. The method of Claim 45, wherein said hydrophobic bonds comprise Si-O-Si-$(CH_3)_3$ bonds.

47. The method of Claim 45, wherein said hydrophobic bonds comprise Si-O-$Si(CH_3)_2$-O-Si bonds.